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DATE: ***September 5, 2003*** COVER SHEET & ***72*** PAGE(S)

CLIENT NUMBER: ***29195-8171US***

RETURN TO: (NAME) ***Melody*** (EXT.) ***6771*** (ROOM NO.) ***4183***

ORIGINAL DOCUMENT(S) WILL BE: ☒ SENT TO USPTO ON MAY 23, 2003 ☐ HELD IN OUR FILES

SENDER:	TELEPHONE:	FACSIMILE:
Melody J. Almberg	*(206) 264-6771*	*206-332-7198*

RECIPIENT:	COMPANY:	TELEPHONE:	FACSIMILE:
Robert Warden	*Technology Center 1700*	*703-308-2920*	*703-872-9394*

RE: ***US Patent No. 6,197,181***
Issue Date: March 6, 2001
US Application No. 09/045,245
Filed: March 20, 2998

Per our conversation, attached please find the Petition to Correct Inventorship. If you have any questions, please do not hesitate to contact our office.

Thank you for your assistance with this matter.

Attorney Docket No. 29195.8171US

Express Mail Label EV343591657US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE PATENT APPLICATION NO.:	6,197,181
APPLICATION NO.:	09/045,245
FILED:	MARCH 20, 1998
ISSUED:	MARCH 6, 2001
FOR:	METHOD FOR ELECTROLYTICALLY DEPOSITING METAL ON A MICROELECTRONIC WORKPIECE

PETITION TO CORRECT INVENTORSHIP ON AN ISSUED PATENT UNDER 37 C.F.R. 1.324(B)

Supervisory Patent Examiner – 1700
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. Request for Certificate of Correction

The applicant hereby petitions for a Certificate of Correction to correct the inventorship of U.S. Patent No. 6,197,181 by adding Thomas Taylor as a co-inventor with Dr. Linlin Chen. The correct inventorship should be Dr. Linlin Chen and Thomas Taylor.

2. Statement from Thomas Taylor to be Added as an Inventor

Please find enclosed a statement from Thomas Taylor in which Mr. Taylor declares that the error in failing to include him as an inventor of subject matter claimed in U.S. Patent No. 6,197,181 occurred without any deceptive intent on his part (Exhibit A).

3. Statement from Linlin Chen Agreeing to Correction of Inventorship

Please find enclosed a statement from Dr. Linlin Chen in which Dr. Chen states that he does not disagree to correcting the inventorship by adding Thomas Taylor as a joint inventor of subject matter claimed in U.S. Patent No. 6,197,181 (Exhibit B).

4. Statement from Assignee Agreeing to Correction of Inventorship

Please find enclosed a statement from Mr. William Freeman, an officer of the assignee of U.S. Patent No. 6,197,181, indicating that Semitool agrees to the change of inventorship in this patent (Exhibit C). Also, please find enclosed assignments from Dr. Chen and Mr. Taylor assigning their rights in U.S. Application Serial No. 10/302,701, which is a continuation of U.S. Application No. 09/045,245, to Semitool, Inc (Exhibit D).

5. U.S. Patent No. 6,197,181 Subject Matter of Pending Litigation

U.S. Patent No. 6,197,181 is the subject matter of separate lawsuits between Semitool, Inc. and each of Novellus, Inc., Applied Materials, Inc., and Ebarra, Inc. The inadvertent omission of Thomas Taylor as an inventor of subject matter claimed in the '181 Patent first came to light during a deposition in the pending lawsuits. The facts relevant to Taylor's contribution to subject matter claimed in the '181 Patent and the lack of deceptive intent in failing to name him as an inventor are set forth below.

A. Taylor Conceived and Performed Seed Layer Repair at Semitool Before the Application for the '181 Patent was Filed

In April 1997, Taylor was a team leader of Semitool's Advanced Technology Group ("ATG") and was responsible for developing new technologies for improving seed layers. (See Exhibit E - Taylor Dep. at 77:12 - 80:16; 120:2-22; and Exhibit F - Dep. Ex. 51.) On April 4, 1997, the ATG discussed Semitool's developments in seed layer technology. (Exhibit G - Dep. Ex. 55.) During this ATG meeting, Taylor presented information about Semitool's efforts to improve and optimize seed layers, which expressly included Taylor's ideas for using an electroless process to enhance or repair seed layers.

(Exhibit H - Dep. Ex. 56 at NOVONLY10010, NOVONLY10012; Exhibit E - Taylor Dep. at 121:20- 122:1.) The seed layers to be enhanced were ultra-thin seed layers having a thickness in the range of 200 to 500 Angstroms. (Exhibit H - Dep. Ex. 56 at NOVONLY10012; Exhibit E - Taylor Dep. at 124:25 - 125:12.) The purpose of the electroless enhancement process was to fix deficiencies, such as voids and discontinuities, in the seed layer before using an electroplating procedure to bulk fill copper into recesses. (Exhibit I - Dep. Ex. 53 at ST3081; Exhibit E - Taylor Dep. at 86:25 - 87:7; 101:2 - 102:1.)

Following the April 4 ATG meeting regarding seed layers, Taylor designed experiments to demonstrate the electroless seed layer enhancement process to Intel, which was a Semitool customer. (Exhibit I - Dep. Ex. 53 at ST3081; Exhibit E - Taylor Dep. at 99:3-24; 124:25 - 125:12.) These experiments and demonstrations of the electroless process conceived by Taylor while employed by Semitool were conducted under a confidentiality agreement between Semitool and Intel. (*See, e.g.,* Exhibit I - Dep. Ex. 53 at ST3084 identifying electroless Experiment 6 as "Semitool Confidential.") On May 1, 1997, Taylor sent a memorandum to Intel describing his "proposal to supplement the step coverage of PVD seed layers by a short electroless Cu deposition process prior to beginning electrolytic plating." (Exhibit I - Dep. Ex. 53 at ST3081.) The purpose of the experiment was to "[d]etermine if marginal PVD seed layer step coverage can be improved by supplementary electroless deposition." (*Id.* at ST3082; *see also* Exhibit J - Dep. Ex. 1053 at ST16468.) According to Taylor, the seed layers were "marginal" because they were "so thin at the bottom as to become intermittently discontinuous or so thin that the plating results were indistinguishable from having a discontinuous seed." (Exhibit E - Taylor Dep. at 101:15-19.) The following day, on May 2, 1997, Taylor presented information about the design of the electroless experiments to Semitool's ATG. (Exhibit K - Dep. Ex. 54; Exhibit E - Taylor Dep. at 112:2-24.) During May 1997, Taylor revised his electroless experiment and sent Intel further memoranda describing the experiment. (Exhibit L - Dep. Ex. 1054; Exhibit E - Taylor Dep. at

139:7 – 140:15; *see also* Exhibit M - Dep. Ex. 1056 at ST20769-70, ST20776; Exhibit E - Taylor Dep. at 140:22 – 145:21.)

By June 30, 1997, Semitool completed the experiments and prepared a report for Intel. (*See* Exhibit N - Dep. Ex. 1000.) The results of the experiment showed that the electroless process designed by Taylor was effective in eliminating voids and discontinuities in the seed layer for structures larger than approximately 0.7 microns wide. (Exhibit N - Dep. Ex. 1000 at ST3064; Exhibit E – Taylor Dep. at 136:24 - 137:23.)

LinLin Chen, the named inventor of the '181 patent, began working for Semitool on April 14, 1997. (Exhibit O - Cross Decl., ¶ 8.) Although Chen was not present at the April 4 ATG meeting, he received a copy of the June 30 report describing the results of the electroless seed enhancement experiment designed by Taylor. (*See* Exhibit N - Dep. Ex. 1000; Exhibit O - Cross Decl., ¶ 8.) Chen received a copy of this report to inform him of Semitool's current activities regarding seed layers and to "solicit [Chen's] feedback on ways that we might improve our development activities." (Exhibit E - Taylor Dep. at 30:22 - 31:5.) Moreover, at ATG meetings or in other discussions at Semitool, Taylor informed Chen of the results of the electroless experiments. (Exhibit E - Taylor Dep. at 112:25 – 114:11.) In late 1997, Chen began focusing on methods to fix deficiencies in seed layers, and on December 22, 1997, he conceived of an electrolytic seed repair process, which is the preferred embodiment of the inventions described in the '181 patent. The application for the '181 patent was filed on March 20, 1998.

B. Taylor was Inadvertently Omitted as a Co-Inventor of the '181 Patent Without Any Deceptive Intent

In mid to late 1997, a number of personnel and organizational changes occurred involving Semitool's ATG and intellectual property department. In mid 1997, Taylor left the ATG and joined Semitool's marketing department. (Exhbit E - Taylor Dep. at 13:7 – 14:2; 95:5-25.) In November, 1997, Mr. Robert Berner,

Corporate Vice President of Technology for Semitool, terminated his employment with Semitool to work for Applied Materials. (Exhibit O - Cross Decl., ¶ 11.) A few months earlier, Semitool's former intellectual property counsel left the company and Mr. Cross, currently Corporate Counsel at Semitool, joined Semitool in September 1997 as a part-time consultant working only three days a week. (Exhibit O - Cross Decl., ¶ 10.) Mr. Cross did not begin working full-time at Semitool until May 1, 1998, more than a month after the application for the '181 patent was filed. (Exhibit O - Cross Decl., ¶ 14.)

As a result of these personnel and organizational changes, Semitool inadvertently lost track of Taylor's work for using an electroless process to repair or enhance thin seed layers. (Exhibit O - Cross Decl., ¶ 14.) Only through discovery taken in this litigation, including Taylor's depositions, did Semitool realize and have an opportunity to confirm that Taylor had made an inventive contribution to the seed repair processes claimed in the '181 patent. (Exhibit O - Cross Decl., ¶ 15.) Because the omission of Taylor as a co-inventor was made without any deceptive intent, Semitool is entitled to have Taylor added as a co-inventor of the '181 patent.

5. Fee under 37 C.F.R. 1.20(b)

Enclosed is a check covering the fee of $130.00 under 37 C.F.R. § 1.20(b).

6. Additional Fees

Please charge any underpayment of fees for common consideration of this petition to Deposit Account No. 50-0665.

Attorney Docket No. 29195.8171US

Respectfully submitted,

Perkins Coie LLP

Date: May 23, 2003

Paul T. Parker
Registration No. 38,264

Enclosures: Exhibits A-O

Correspondence Address:
Customer No. 25096
Perkins Coie LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 583-8888

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www.perkinscoie.com

DATE: ***September 23, 2003*** COVER SHEET & ***1*** PAGE(S)

CLIENT NUMBER: ***29195-8171***

RETURN TO: (NAME) ***Melody*** (EXT.) ***6771*** (ROOM NO.) ***4183***

ORIGINAL DOCUMENT(S) WILL BE: ☐ SENT TO YOU ☒ HELD IN OUR FILES

SENDER:	TELEPHONE:	FACSIMILE:
Paul T. Parker	***206-359-3258***	***206-332-7198***

RECIPIENT:	COMPANY:	TELEPHONE:	FACSIMILE:
Roy King	***USPTO***	***703-308-1146***	***703-872-9593***

RE: ***Patent No. 6,197,181***
Issued: March 6, 2001
Title: METHOD FOR ELECTROLYTICALLY DEPOSITING METAL ON A MICROELECTRONIC WORKPIECE

Per our conversation, attached please find Declaration of Inventor's Residence.

Attorney Docket No. 29195-8171US
Semitool Ref No. P98-0025

I hereby certify that this correspondence is being transmitted via facsimile to the United States Patent and Trademark Office at (703) 872-9593, on:

Date: 9/23/02 By: Melody J. Almberg
Melody J. Almberg

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE PATENT NO. : 6,197,181
APPLICATION NO.: 09/045,245
FILED: MARCH 20, 1998
ISSUED: MARCH 6, 2001
FOR: **METHOD FOR ELECTROLYTICALLY DEPOSITING METAL ON A MICROELECTRONIC WORKPIECE**

STATEMENT OF INVENTOR'S RESIDENCE

Examiner R. King
Supervisory Patent Examiner (1742)
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner King:

Thomas Taylor's residence, to the best of our knowledge, is in Worcester County, Massachusettes.

Respectfully submitted,
Perkins Coie LLP

Date: 9/23/03

Paul T. Parker
Registration No. 38,264

Correspondence Address:
Customer No. 25096
Perkins Coie LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 583-8888

Exhibit A

Attorney Docket No. 291958171US2
Semitool Ref No. P98-0025US3

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Linlin Chen and Thomas Taylor
Application No. and related Patent No.	:	10/302,711 and U.S. Patent No. 6,197,181
Filed	:	November 22, 2002
For	:	APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE
	Docket No. :	291958171US2
	Date :	November 22, 2002

Commissioner for Patents
Washington, DC 20231

STATEMENT OF THOMAS TAYLOR REGARDING JOINT INVENTORSHIP

Sir:

I, Thomas Taylor, hereby state that the error in failing to include me as an inventor of certain subject matter claimed in U.S. Patent No. 6,197,181 occurred without any deceptive intent on my part.

April 25, 2003
Date

/s/
Thomas Taylor

Exhibit B

Attorney Docket No. 291958171US2
Semitool Ref No. P98-0025US3

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Linlin Chen and Thomas Taylor
Application No. and related Patent No.	:	10/302,711 and U.S. Patent No. 6,197,181
Filed	:	November 22, 2002
For	:	APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE
Docket No.	:	291958171US2
Date	:	November 22, 2002

Commissioner for Patents
Washington, DC 20231

STATEMENT OF LINLIN CHEN REGARDING JOINT INVENTORSHIP

Sir:

I, Linlin Chen, hereby state that I have no disagreement in regards to the joint inventorship of me and Thomas Taylor with respect to the claimed subject matter for the above-identified application set forth in the Preliminary Amendment filed on November 22, 2002, and in certain claimed subject matter in U.S. Patent No. 6,197,181.

2/10/2003
Date

Linlin Chen

Exhibit C

Atto. Docket No. 29195.8171US00

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE PATENT APPLICATION NO.:	6,197,181
APPLICATION NO.:	09/045,245
FILED:	MARCH 20, 1998
ISSUED:	MARCH 6, 2001
FOR:	**METHOD FOR ELECTROLYTICALLY DEPOSITING METAL ON A MICROELECTRONIC WORKPIECE**

Statement by Assignee Regarding Joint Inventorship and Certification Under 37 C.F.R. § 3.73(b)

Supervisory Patent Examiner - 1700
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, the undersigned, acting on behalf of the Assignee of the entire right, title and interest in the above-identified patent, by virtue of Assignments filed by Linlin Chen and Thomas Taylor in U.S. Application No. 10/302,711, which is a continuation of U.S. Patent No. 6,197,181, hereby state that the Assignee agrees to the change in inventorship in U.S. Patent No. 6,197,181 to include Linlin Chen and Thomas Taylor.

In accordance with 37 C.F.R. § 3.73(b), I hereby certify that I am empowered to act on behalf of the Assignee. To the best of my knowledge and belief, title is in the Assignee, as evidenced by the Assignments noted above.

I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, USC § 1001 and that such willful false statements may jeopardize the validity of this application or any patent resulting therefrom.

ASSIGNEE: Semitool, Inc.

Attor..., Docket No. 29195.8171US00

Signature: William A. Freeman

Typed Name: William Freeman

Title: Senior Vice President, Finance and CFO

Date:

Address: P. O. Box 7010, Kalispell, MT 59904-0010

Exhibit D

USSN 10/302,711

Attorney Docket: 29195-8171US2
Semitool Ref No. P98-0025US3

ASSIGNMENT

THIS ASSIGNMENT is by Linlin Chen and Thomas Taylor (the "Assignors"), residing at 3213 Placid Springs Lane, Plano TX 75025, and 308 SW Montgomery Street #206, Portland, OR 97201, respectively. We Assignors have invented one or more certain inventions described in a United States Patent Application entitled APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE (the "Application") and ☐ executed concurrently herewith; or ☒ filed on November 22, 2002 as Application No. 10/302,711 (the "Invention(s)"). We Assignors authorize the Assignee, identified below, or its representatives to insert the filing date and application number of the Application when known.

Semitool, Inc., a corporation of the State of Montana having a place of business at 655 West Reserve Drive, Kalispell MT 59901 ("Assignee"), desires to acquire the entire right, title and interest in and to the Invention(s) and the Application, and in and to any patents (collectively, "Patents") that may be granted for the Invention(s) in the United States or in any foreign countries.

For valuable consideration, the receipt and sufficiency of which we acknowledge, Assignors hereby sell, assign, and transfer to Assignee, its successors, legal representatives and assigns, the entire right, title and interest in and to: the Invention(s), the Application, and any Patents; any divisions, continuations, and continuations-in-part of the Application and any other application claiming priority rights from the Application; any reissues, reexaminations, or extensions of any and all Patents; the right to file foreign applications directly in the name of Assignee; and the right to claim priority rights deriving from the Application (collectively, the "Rights"). Assignors warrant that they are joint owners of the Rights, and that the Rights are unencumbered. Assignors also agree to not sign any writing or do any act conflicting with this assignment, and, without further compensation, sign all documents and do such additional acts as Assignee deems necessary or desirable to: perfect Assignee's enjoyment of the Rights; prepare and prosecute the Application or any other applications for Patents; conduct proceedings regarding the Rights, including any litigation or interference proceedings; or perfect or defend title to the Rights. Assignors request the Commissioner of Patents to issue any Patent of the United States that may be issued on the Invention(s) to Assignee. This Assignment may be executed in counterparts.

USSN 10/302,711 Attorney Docket: 99999-9999

Date: 9/10/2003 Linlin Chen

STATE OF _____

COUNTY OF _____

On _____ before me personally appeared Linlin Chen, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

(Seal) _____ Signature

* * * * * * * *

Date: _____ Thomas Taylor

STATE OF _____

COUNTY OF _____

On _____ before me personally appeared Thomas Taylor, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

(Seal) _____ Signature

* * * * * * * *

USSN 10/302,711

Attorney Docket: 29195-8171US2
Semitool Ref No. P98-0025US3

ASSIGNMENT

THIS ASSIGNMENT is by Linlin Chen and Thomas Taylor (the "Assignors"), residing at 3213 Placid Springs Lane, Plano TX 75025, and 308 SW Montgomery Street #206, Portland, OR 97201, respectively. We Assignors have invented one or more certain inventions described in a United States Patent Application entitled APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE (the "Application") and ☐ executed concurrently herewith; or ☒ filed on November 22, 2002 as Application No. 10/302,711 (the "Invention(s)"). We Assignors authorize the Assignee, identified below, or its representatives to insert the filing date and application number of the Application when known.

Semitool, Inc., a corporation of the State of Montana having a place of business at 655 West Reserve Drive, Kalispell MT 59901 ("Assignee"), desires to acquire the entire right, title and interest in and to the Invention(s) and the Application, and in and to any patents (collectively, "Patents") that may be granted for the Invention(s) in the United States or in any foreign countries.

For valuable consideration, the receipt and sufficiency of which we acknowledge, Assignors hereby sell, assign, and transfer to Assignee, its successors, legal representatives and assigns, the entire right, title and interest in and to: the Invention(s), the Application, and any Patents; any divisions, continuations, and continuations-in-part of the Application and any other application claiming priority rights from the Application; any reissues, reexaminations, or extensions of any and all Patents; the right to file foreign applications directly in the name of Assignee; and the right to claim priority rights deriving from the Application (collectively, the "Rights"). Assignors warrant that they are joint owners of the Rights, and that the Rights are unencumbered. Assignors also agree to not sign any writing or do any act conflicting with this assignment, and, without further compensation, sign all documents and do such additional acts as Assignee deems necessary or desirable to: perfect Assignee's enjoyment of the Rights; prepare and prosecute the Application or any other applications for Patents; conduct proceedings regarding the Rights, including any litigation or interference proceedings; or perfect or defend title to the Rights. Assignors request the Commissioner of Patents to issue any Patent of the United States that may be issued on the Invention(s) to Assignee. This Assignment may be executed in counterparts.

USSN 10/302,711 Attorney Docket: 99999-9999

Date:_____ _____
Linlin Chen

STATE OF _____

COUNTY OF _____

On _____ before me personally appeared Linlin Chen, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

(Seal) _____
Signature

* * * * * * * * *

Date: April 25, 2003 _____
Thomas Taylor

STATE OF Massachusetts

COUNTY OF Middlesex

On April 25, 2003 before me personally appeared Thomas Taylor, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

(Seal) M. Frank Rizzilli
Signature
Expires June 12, 2009

* * * * * * * * *

Exhibit E

CONDENSED TRAN. . .RIPT

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

SEMITOOL, INC.,
Plaintiff,

vs. No. 16-01-06060

NOVELLUS SYSTEMS, INC.,
Defendant.

HIGHLY CONFIDENTIAL

VIDEOTAPED DEPOSITION OF

THOMAS TAYLOR

VOLUME II

October 23, 2002
9:15 a.m.

6011 SW Second Avenue
Suite 1600
Portland, Oregon

Carol Ann Nevarez, Certified Shorthand Reporter for Oregon

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF OREGON

SEMITOOL, INC., Plaintiff, vs. APPLIED MATERIALS, INC., Defendant.) No. 01-CV-1066-BR

SEMITOOL, INC., Plaintiff, vs. EBARA CORPORATION and EBARA TECHNOLOGIES, INC., Defendants.) No. 01-CV-873-BR

SEMITOOL, INC., Plaintiff, vs. NOVELLUS SYSTEMS, INC., Defendant.) No. 01-CV-874-BR

HIGHLY CONFIDENTIAL

****CONTAINS****

HIGHLY CONFIDENTIAL

INFORMATION

VIDEOTAPED DEPOSITION OF THOMAS TAYLOR

Taken in behalf of Defendant Novellus Systems, Inc.

March 25, 2002

Portland, Oregon

BE IT REMEMBERED that the videotaped deposition of THOMAS TAYLOR was taken in behalf of Defendant Novellus Systems, Inc., pursuant to the Federal Rules of Civil Procedure, before Bonita J. Alexander, Certified Shorthand Reporter for Oregon, on Monday, the 25th day of March, 2002, in the law offices of Perkins Coie LLP, 1211 S.W. Fifth Avenue, Suite 1500, Portland, Oregon, commencing at the hour of 9:50 a.m.

APPEARANCES

PERKINS COIE LLP
By: Mr. Jerry A. Riedinger and Mr. Paul T. Fortino, appearing in behalf of the Plaintiff;

WEIL, GOTSHAL & MANGES LLP
By: Mr. Jared Bobrow, appearing in behalf of Defendant Applied Materials, Inc.;

FISH & NEAVE
By: Mr. Terrence J.P. Kearney, appearing in behalf of Defendant Ebara Corporation;

HIGHLY CONFIDENTIAL

IRELL & MANELLA LLP
By: Mr. Roman Melnik, appearing in behalf of Defendant Novellus Systems, Inc.

SEMITOOL, INC.
By: Mr. Harry Cross, In-House Counsel.

ALSO PRESENT
William Thoma, Limelight Video Productions

INDEX

DEPOSITION OF THOMAS TAYLOR

—oOo—
*** NO EXHIBITS MARKED ***
—oOo—

THE VIDEOGRAPHER: This is Volume 1, tape 1 in the deposition of Tom Taylor, in the matter of Semitool vs. Novellus Systems, Case No. 01-CV-874-BR; also Semitool vs. Applied Materials, 01-CV-1066-BR; and also Semitool vs. Ebara Technologies, Inc., 01-CV-873-BR. Today's date is March 25th, 2002. The time on the video monitor is 9:50 a.m. The video operator today is William Thoma, contracted by Legalink Los Angeles, at 16830 Ventura Boulevard, Encino, California. 09:50:14 09:50:16 09:50:16 09:50:21 09:50:27 09:50:34 09:50:41 09:50:45 09:50:50 09:50:53 09:50:58

This video deposition is taking place at Perkins Coie, 1211 Southwest Fifth, Portland, Oregon, and was noticed by Roman Melnik of Irell & Manella. 09:51:00 09:51:02 09:51:06 09:51:09

Counsel, please voice identify yourselves and state whom you represent. 09:51:11 09:51:13

MR. MELNIK: Roman Melnik of Irell for Novellus Systems. 09:51:15 09:51:18

MR. BOBROW: Jared Bobrow of Weil, Gotshal for Applied Materials. 09:51:19 09:51:20

MR. KEARNEY: Terry Kearney of Fish & Neave, for Ebara Corporation. 09:51:23 09:51:26

MR. RIEDINGER: Jerry Riedinger from Perkins Coie for Semitool. And also with me is 09:51:27 09:51:28

Mr. Paul Fortino from Perkins Coie, and Mr. Harry Cross, corporate counsel for Semitool. 09:51:32 09:51:35
THE VIDEOGRAPHER: The court reporter is Bonita Alexander of Beovich Walter & Friend. 09:51:38 09:51:39
Would the court reporter please swear in the witness. 09:51:42 09:51:43
09:51:44

THOMAS TAYLOR

called as a witness in behalf of Defendant Novellus Systems, Inc., being first duly sworn, is examined and testifies as follows:

EXAMINATION

BY MR. MELNIK: 09:51:52

Q. Mr. Taylor, would you please state your full name and address for the record, please. 09:51:53 09:51:55
A. My name is Thomas Charles Taylor. My address is 0308 Southwest Montgomery, Apartment No. 206, Portland, Oregon. 09:51:57 09:51:59 09:52:04
Q. Mr. Taylor, are you being represented by a lawyer in today's deposition? 09:52:07 09:52:11
A. No. I'm here without the benefit of counsel. 09:52:12 09:52:14
Q. You have -- do you understand that you have the right to bring a lawyer to the deposition? 09:52:16 09:52:16

6

A. I do. 09:52:20
Q. And you would like to proceed without a lawyer? 09:52:21 09:52:23
A. I would. 09:52:23
Q. At some point prior to today's deposition, were you contacted by the Perkins Coie law firm about representing you at this deposition? 09:52:23 09:52:31 09:52:35
A. Perkins Coie offered to represent me, as did, in fact, the attorneys for Shipley Company, with whom I was employed following my tenure at Semitool. 09:52:37 09:52:42 09:52:45 09:52:49
Q. And what was your response? 09:52:50
A. At the time I appreciated the offer, did not make a commitment, and chose effectively about two weeks ago to proceed without official representation. 09:52:50 09:52:54 09:52:58 09:53:01
Q. Mr. Taylor, can you please tell me about your educational background, beginning with college, please. 09:53:01 09:53:14 09:53:20
A. Certainly. I graduated from the University of Utah in 1984 with a baccalaureate in chemical engineering, a bachelor of science in chemical engineering, proceeded in 1989 to pursue a master's in materials science at the University of Minnesota while employed at Cray Research, chose to take a position working in Japan prior to completing thesis work, so that was incomplete. 09:53:20 09:53:22 09:53:27 09:53:31 09:53:35 09:53:37 09:53:42 09:53:45
I'm currently in the Ph.D. program at Portland State University, in the discipline called systems science. 09:53:46 09:53:49 09:53:52
Q. Since you didn't have a lawyer, who told you about -- Let me ask this. Is this your first deposition? 09:53:54 09:54:05 09:54:07
A. First ever. 09:54:07
Q. I guess I should give you a little bit of background on how these things work. You notice to the left there's a court reporter who is taking down what you and I are saying, and there's also a videographer over there videotaping you. The most important part of this is because we're doing a written transcript, it's important not to do what normal people do, which is to nod and make nonverbal -- and give nonverbal answers. It's important to say yes or no, rather than huh-uh, uh-huh, or something like that. 09:54:08 09:54:11 09:54:13 09:54:15 09:54:18 09:54:22 09:54:24 09:54:28 09:54:32 09:54:35 09:54:38
A. If you catch me, please correct me. 09:54:40
Q. I will try. And vice versa. I do it, too. 09:54:42 09:54:45
Also, it's important so that we can all go home at a reasonable hour, including most importantly you, that you listen carefully to the questions that I ask and answer those questions so that I don't have to repeat my questions several times, because the way people normally speak to each other is they listen to the context of the question and respond to the context. Lawyers frequently, not being people, don't pose questions that way, they tend to pose questions in a very particular narrow way, and it's important to listen to the exact questions being asked before you answer. 09:54:46 09:54:51 09:54:53 09:54:55 09:55:02 09:55:04 09:55:08 09:55:10 09:55:14 09:55:18 09:55:21 09:55:23
A. I understand. 09:55:24
Q. Okay. So can you please tell me now your employment history, starting with your first job and going up to your time at Shipley. 09:55:24 09:55:36 09:55:42
A. Yes. The first job -- the first job in this industry was in 1977, at Motorola, what was at that time called NMOS, prior to the formation of their silicon product sector. 09:55:44 09:55:50 09:55:57 09:55:59
Following that, worked for six years at National Semiconductor in Salt Lake City in both engineering and production management roles. 09:56:01 09:56:06 09:56:13
Q. When did you leave Motorola? 09:56:16
A. 19 -- late 1976. 09:56:17
Q. Go ahead, please. 09:56:20
A. I was at National Semiconductor through 09:56:22

9

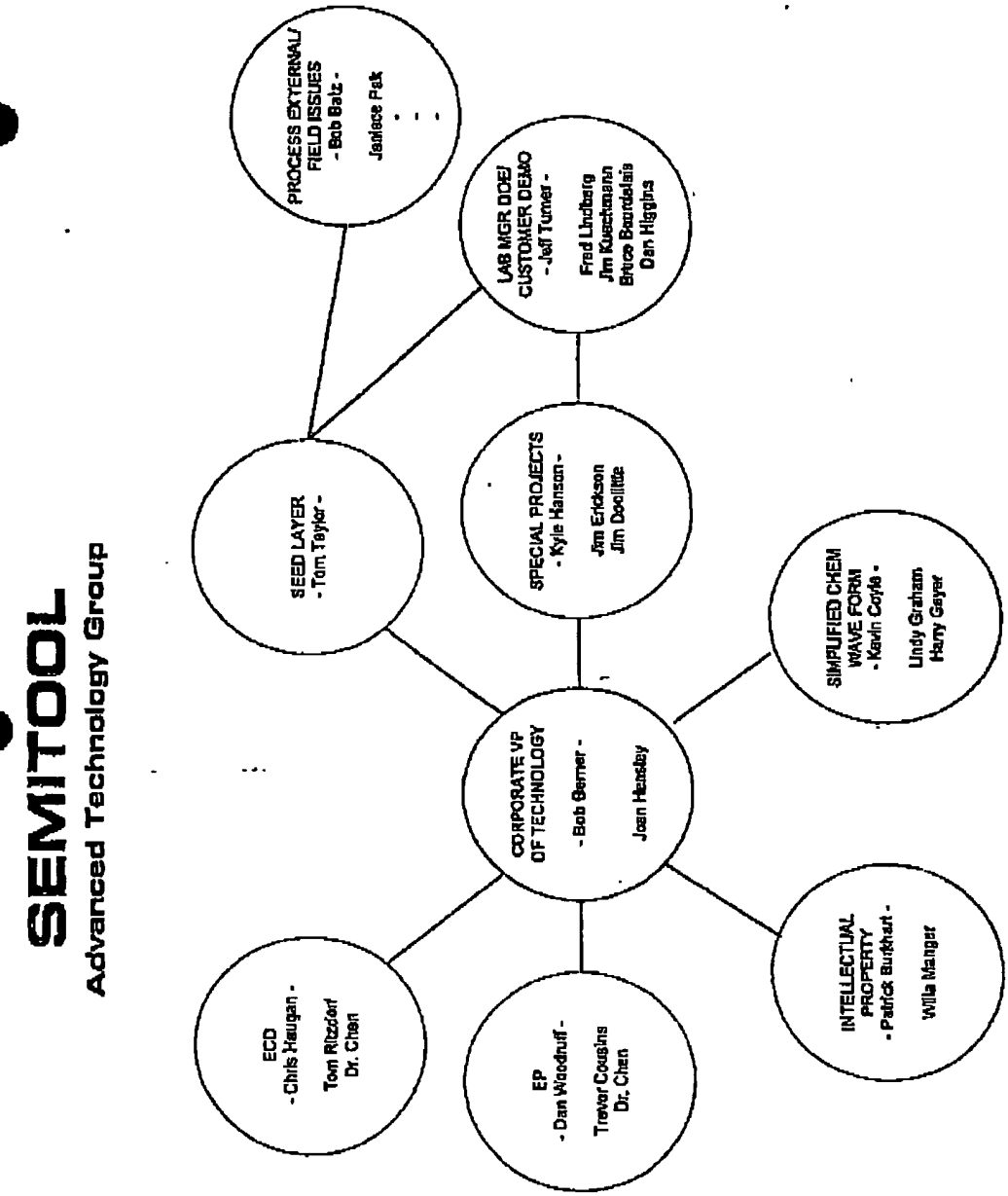
1984, at the time that I got my degree, if you 09:56:25
recall, and went to work for an organization called 09:56:29
FSI for a very short period of time, six months, was 09:56:34
recruited away to Sperry, in Eagan, Minnesota, as a 09:56:38
process development engineer. 09:56:44
Sperry was acquired by Burroughs. I went 09:56:49
to Cray Research in Chippewa Falls, Wisconsin from 09:56:53
1986, roughly, to 1989. 09:57:00
In 1989 I took a position with a company 09:57:06
called Ramtron International Corporation. 09:57:09
You smile. 09:57:13
Q. No, I'm only smiling because you have a 09:57:13
rather long employment – unusually long employment 09:57:17
history. 09:57:20
A. It has been 24 years, but you're right, 09:57:21
there are a number. 09:57:23
Q. Please go ahead. 09:57:24
A. At Ramtron my position was to lead a team 09:57:25
developing a specialty DRAM fabrication technology 09:57:28
for a company called NMBS Semiconductor in Tateyama, 09:57:34
Japan. That was an 18-month stint. 09:57:40
At the conclusion of that, I went to work 09:57:43
for Ramtron in Colorado Springs for – until 1996. 09:57:45
In the spring of 1996, took the position with 09:57:58
Semitool in Kalispell, Montana, was there until the 09:58:01

spring of 1999, at which time I went to work for 09:58:04
Rohm & Hass Company and its subsidiaries, Shipley 09:58:11
and Rodel. 09:58:15
Q. Now, do you remember exactly when in 1996 09:58:16
you joined Semitool? 09:58:21
A. I do recall – I'm sorry, I could have 09:58:23
brought that, but it was the autumn of 1996. 09:58:26
Q. Autumn of 1996. And do you remember 09:58:28
exactly when during the autumn of 1996? 09:58:31
A. I'm sorry, I don't remember precisely, 09:58:34
exactly what month it was. 09:58:37
Q. Do you remember early versus late autumn? 09:58:39
A. I remember that there was frost on the 09:58:41
pumpkins. I was in my temporary – this was perhaps 09:58:45
summertime, late summer as opposed to fall, but that 09:58:51
was approximately when it was. 09:58:54
Q. Late summer-early fall? 09:58:57
A. Yeah. 09:58:59
Q. Or possibly a little later? 09:58:59
A. (Witness nods head.) 09:59:01
Q. And do you remember exactly when you left 09:59:01
Semitool? 09:59:09
A. My recollection is the end of – beginning 09:59:09
of April of 1999. 09:59:12
Q. I think you described this a little bit 09:59:22

already, but just – I was taking notes and perhaps 09:59:23
I wasn't listening as carefully as I should have 09:59:26
been. Can you describe in a little more detail your 09:59:28
work at Ramtron for me. 09:59:31
A. At Ramtron I started as the manager of 09:59:33
process development, took a role after approximately 09:59:36
two years as the director of technology alliances, 09:59:44
and held that position until I departed. This is in 09:59:47
Colorado Springs, of course. 09:59:51
Q. And as director of technology alliances, 09:59:55
was that primarily an R and D job or primarily a 09:59:58
marketing-type job? 10:00:02
A. It was an add mixture of the two. It was 10:00:03
a role in which I was responsible for developing 10:00:06
contractual arrangements between Ramtron and 10:00:13
large-scale manufacturers for the transfer of 10:00:16
Ramtron's proprietary ferroelectric memory 10:00:19
technology, which required a fairly in-depth 10:00:24
knowledge as to the details of that technology and 10:00:26
how it might be implemented in the CMOS baseline 10:00:28
structures of a variety of partners. And it also, 10:00:35
of course, required a certain amount of technical 10:00:38
marketing as well. 10:00:40
Q. Did your responsibilities at Ramtron 10:00:46
relate in any way to electroplating or electroless 10:00:50

deposition? 10:00:57
A. None. 10:00:57
Q. I'm sorry, was the answer "none"? 10:00:59
A. The answer was none. The answer was that 10:01:00
none of those responsibilities related to 10:01:04
electroplating or electroless technology. 10:01:07
Q. When you started at Semitool, whatever the 10:01:18
time frame was, early fall of 1996, do you recall 10:01:22
what your first job responsibility was? 10:01:29
A. At? 10:01:32
Q. Semitool. 10:01:34
A. Yes. My responsibilities were as the 10:01:36
process development manager, and I was tasked with 10:01:38
overseeing the activities of a group of process 10:01:44
development engineers working in both electroplating 10:01:49
and in single-substrate wet chemical processing, 10:01:51
cleaning solvent and acid cleaning and so forth, 10:01:55
etching. 10:01:58
Q. And for how long did you remain process 10:02:16
development manager at Semitool? 10:02:20
A. For approximately nine months, and – 10:02:22
well, approximately nine months. 10:02:27
Q. And when did you change positions, and 10:02:28
what was your next position? 10:02:33
A. Approximately nine months after I arrived, 10:02:34

Exhibit F



Bob Berner

April 9, 1997

Ex. 51

SEMITOOL®

Advanced Technology Group

Process:

- Simple Chemistry
- Waveforms
- Analysis
- Chem. Analysis Replenishment

Film Quality Vs. Reactor Geometry:

- Modeling
- Experiments

Automation:

- Reactor Design

SEMITOOL®

Advanced Technology Group

- Process
- Film Quality Vs. Reactor
- Automation

Exhibit G

SEMITOOL®

Advanced Technology Group

655 West Reserve Drive, PO Box 7010, Kalispell, MT 59904 Phone: 406-752-2107 Fax: 406-752-5622

To: Bob Berner, Chris Haugan, Dan Woodruff, Kevin Coyle, Tom Taylor, Kyle Hanson, Jeff Turner, Bob Batz, Patrick Burkhart

From: Joan Hensley

Date: 2-Apr-97

Subject: Meeting Agenda, April 4, '97

cc: ATG Group, Ray Thompson, Greg Perkins, John Sullivan

Agenda

Meeting: ATG Meeting
Executive Lunch Room East & West
Friday, April 4, 1997
8:30 am

Presentations: Team leaders will each have approximately 20 min. for their presentation. The presentation will include their project description, tentative schedule, and the expected results to include the definition of the completion of the project/Criteria.

	Presenter	Project
8:30 - 8:50 am:	Chris Haugan	Modeling
8:50 - 9:10 am:	Dan Woodruff	Polish
9:10 - 9:30 am:	Kevin Coyle	Wave Form/Simplified Chem
9:30 - 9:50 am:	Tom Taylor	Seed Layer Development
9:50 - 10:10 am:	Kyle Hanson	Special Projects
10:10 - 10:20 am:	Bob Batz	Solder
10:20 - 10:40 am:	Patrick Burkhart	Intellectual Property

E. 55

Exhibit H

Tom Taylor

Ex. 56

Barrier Layer Optimization

- Materials
  - Ti/TiN, Ta, TaN, WN, …
- Deposition Method
  - PVD vs. CVD
- Selection Criteria
  - Cu Diffusivity at Elevated Temperatures
  - Adhesion to Dielectrics
  - Adhesion to ECD Seed Layer
  - Resistivity
  - Galvanic Reactivity With Cu
  - Morphology / Crystallinity

Seed Layer Optimization

- Deposition Method
  - PVD vs. CVD
- Major Issues
  - Step Coverage
  - Thickness Requirements
    - Continuity in high aspect-ratio features
    - "Pinch-off" in throats of trench/via patterns
    - Scaling for current density effects vs. substrate diameter
    - Throughput balancing
  - Nucleation Site Density
    - Influence on ECD Cu morphology / grain size distribution

PVD vs. CVD for Barrier/Seed

- PVD Methods
  - "Conventional", collimated-beam, metal ion sputter
  - High temperature process for step coverage?
- CVD Methods
  - Thermal CVD vs. Plasma-Enhanced CVD (PECVD)
  - Precursor cost and efficiency
  - Better step coverage than PVD
  - Environmental concerns -- exhaust scrubbers
  - System cleaning requirements
- Combination Methods -- AMAT?

Seed Layer Enhancement

- Electroless Cu on Thin PVD/CVD Cu Seed
  - No Applied Current Eliminates "Deplating" Danger
  - Less Sensitive to Initial Seed Layer Discontinuities
  - Initial Seed Layer Requirements 200 - 500 A
  - Flexibility to Modify Pre-ECD Seed for Variations in Device Type, Substrate Size, …
- Modified Electroplating
  - "Strike Bath" Concept
  - Electrolyte/Plating Conditions Optimized for Early Film Growth

4-4-97

Seed Layer Elimination

- Electroless Cu Deposition on Catalyzed Barrier
  - Catalysts Include : Cu (naturally), Au, Pd, Pt, ?
  - Literature Includes Data on Catalytization of TiN by Immersion in PdCl or PtCl Baths
- Direct-to-Barrier ECD Plating
  - Identify Materials Which Are "Dual Function" -- Good Cu Diffusion Barrier and Platable with Good Uniformity and Adhesion
  - First Attempts w/ Ir and IrO2
  - Modified TiN ?

Taylor 9-9-97

Project Schedule

Task	Q2/97			Q3/97			Q4/97		
	4/97	5/97	6/97	7/97	8/97	9/97	10/97	11/97	12/97
Conventional Seed Layer Optimiztion									
PVD vs. CVD									
Thickness, Morphology									
Seed Layer Enhancement									
Electroless Cu									
Strike Bath									
Seed Layer Elimination									
Electroless on Barrier									
ECD on Barrier									

Taylor 4.4.97

Exhibit I

SEMITOOL®

Metallization Process Group
655 West Reserve Drive, PO Box 7010, Kalispell, MT 59904 Phone: 406-752-2107 Fax: 406-752-5522

FAX COVER SHEET

To:	Chun Mu	Fax#	408-765-2949
From:	Thomas Taylor		
Date:	May 1, 1997		
Subject:	Experiment 5 & 6 Proposals	Pages Including Cover:	4

Dear Chun,

Thanks for hosting yet another fascinating meeting. You must know how much I love being shown experimental observations that I can't explain, since you manage to surprise me every time we get together.

I appreciate being given copies of the colorized SEM pastiches showing the evolution of the Cu deposition in a range of trench widths, and the unmanipulated photos from which the composites were produced. I have had a chance to review these with a number of he process engineers here in Kalispell, and we've tended to consensus on the probable mechanism for the different film growth behavior demonstrated by the various power supply settings (DC, FWD, PR). In general, we agree that the likely hypothesis is an interaction between the plating waveform (or peak current density) and the adsorption of the organic additives present in the electrolyte, particularly the leveller/suppressant agents.

As agreed, I have roughly defined experiments intended to increase our mutual knowledge of the mechanisms at work. As before, Semitool will supply the electroplating process, Intel will supply the wafers, and I will personally supply the dumbfounded looks when the results are presented.

The first experiment is directly related to the results discussed on Monday, April 28th, and should be self-explanatory. The second experiment is related to my proposal to supplement the step-coverage of PVD seed layers by a short electroless Cu deposition process prior to beginning electrolytic plating; if you are at all interested, we may choose to pursue this either immediately or at some later date.

Please call if you have any questions or suggestions on how the proposed experiments can be improved.

Very Best Regards,

T. Taylor

Experiment 5 (In our ongoing series)
Evaluate interactions between the plating waveforms and peak current densities with the brightener and leveller/suppressant agents in the electrolyte.

Barrier : Ta or TaN, thickness = 150A

Seed layer : PVD Cu, thickness = 1500A

Experiment conducted as full factorial, with 5 electrolyte solutions and 9 plating power conditions. Five replicate wafers to be run (FWD pulse plating at standard current density, one at each bath composition). Total wafers required = [(9*5) + 5] = 50 wafers.

Bath Chemistries To Be Evaluated :

1) "STI Basic Bath" (CuSO4/H2SO4/H2O)
2) Enthone-OMI CU BATH M with no additives
3) Enthone-OME CU BATH M with brightener/carrier agents only at nominal working strength
4) Enthone-OME CU BATH M with leveller/suppressant agents only at nominal working strength
5) Enthone-OME CU BATH M with both additive packages at nominal working strength as control

Plating Power Supply Setpoints To Be Evaluated :

For all conditions, peak cathodic current densities of 23mA/cm2, 30.5mA/cm2, and 38mA/cm2
For all conditions, total plated thickness of 4000 A (approx. 6.4 Amp min)
Conditions : DC plating, FWD pulse, Pulse Reverse

Please see the attached spreadsheet labelled EXPERIMENT 5 for the run-by-run schedule.

Experiment 6
Determine if marginal PVDseed layer step coverage can be improved by supplementary electroless deposition.

Barrier: Ta or TaN, 150A thickness

Seed layer : PVD Cu; thickness splits : 500A, 1000A, 1500A

Number of wafers per seed layer thickness : 15 (to allow for some trial-and-error process development in the following electroless deposition process)

Electroless deposition process targets : Add 500A, 1000A, 1500A of Cu (up to 5 wafers each per seed thickness)

Total number of wafers : 45

Following electroless deposition, one wafer per seed layer /electroless supplement thickness combination will be sectioned for SEM analysis. The remaining wafers will be processed through a baseline Cu electroplating recipe, consisting of Enthone-OMI CU BATH M with additives, and FWD pulse plating at nominal parameters. Wafers will be sectioned to determine gap fill characteristics and grain morphology. XRD should be performed to determine crystallinity and orientation.

Please see the attached spreadsheet labelled EXPERIMENT 6 for the run-by-run schedule.

DC AND 9.2 FWD
6.8 AND 9.0 9.2 9.0
5 BATHS 2 3 BATHS

EXPERIMENT 5

Bath Types :
1) "STI Basic Bath"
2) CU BATH M with no additives
3) CU BATH M with brightener/carrier only
4) CU MATH M with leveller/suppressor only
5) CU BATH M with all additives (brighteners and levellers)

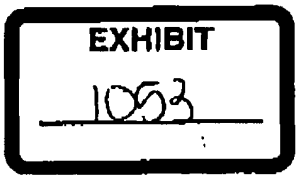
Wafer #	Bath Type	Applied Power	Peak Current
1	1	DC	6.8A
2	1	DC	9.0A
3	1	DC	11.2A
4	1	FWD	6.8A
5	1	FWD	9.0A
6	1	FWD	11.2A
7	1	PR	6.8A
8	1	PR	9.0A
9	1	PR	11.2A
10	2	DC	6.8A
11	2	DC	9.0A
12	2	DC	11.2A
13	2	FWD	6.8A
14	2	FWD	9.0A
15	2	FWD	11.2A
16	2	PR	6.8A
17	2	PR	9.0A
18	2	PR	11.2A
19	3	DC	6.8A
20	3	DC	9.0A
21	3	DC	11.2A
22	3	FWD	6.8A
23	3	FWD	9.0A
24	3	FWD	11.2A
25	3	PR	6.8A
26	3	PR	9.0A
27	3	PR	11.2A
28	4	DC	6.8A
29	4	DC	9.0A
30	4	DC	11.2A
31	4	FWD	6.8A
32	4	FWD	9.0A
33	4	FWD	11.2A
34	4	PR	6.8A
35	4	PR	9.0A
36	4	PR	11.2A
37	4	DC	6.8A
38	4	DC	9.0A
39	4	DC	11.2A
40	5	FWD	6.8A
41	5	FWD	9.0A
42	5	FWD	11.2A
43	5	PR	6.8A
44	5	PR	9.0A
45	5	PR	11.2A
46	1	FWD	6.8A
47	2	FWD	6.8A
48	3	FWD	6.8A
49	4	FWD	6.8A
50	5	FWD	6.8A

3 of 4

Experiment 6

Wafer #	Seed Layer Thickness	Electroless Cu Thickness	Post-processing
1	500 A	500 A	SEM Section
2	500 A	500 A	Electroplate (1.0m) and SEM Section
3	500 A	500 A	Electroplate (1.0m) and SEM Section
4	500 A	500 A	Electroplate (1.0m) and SEM Section
5	500 A	500 A	Electroplate (1.0m) and SEM Section
6	500 A	1000 A	SEM Section
7	500 A	1000 A	Electroplate (1.0m) and SEM Section
8	500 A	1000 A	Electroplate (1.0m) and SEM Section
9	500 A	1000 A	Electroplate (1.0m) and SEM Section
10	500 A	1000 A	Electroplate (1.0m) and SEM Section
11	500 A	1500 A	SEM Section
12	500 A	1500 A	Electroplate (1.0m) and SEM Section
13	500 A	1500 A	Electroplate (1.0m) and SEM Section
14	500 A	1500 A	Electroplate (1.0m) and SEM Section
15	500 A	1500 A	Electroplate (1.0m) and SEM Section
16	1000 A	500 A	SEM Section
17	1000 A	500 A	Electroplate (1.0m) and SEM Section
18	1000 A	500 A	Electroplate (1.0m) and SEM Section
19	1000 A	500 A	Electroplate (1.0m) and SEM Section
20	1000 A	500 A	Electroplate (1.0m) and SEM Section
21	1000 A	1000 A	SEM Section
22	1000 A	1000 A	Electroplate (1.0m) and SEM Section
23	1000 A	1000 A	Electroplate (1.0m) and SEM Section
24	1000 A	1000 A	Electroplate (1.0m) and SEM Section
25	1000 A	1000 A	Electroplate (1.0m) and SEM Section
26	1000 A	1500 A	SEM Section
27	1000 A	1500 A	Electroplate (1.0m) and SEM Section
28	1000 A	1500 A	Electroplate (1.0m) and SEM Section
29	1000 A	1500 A	Electroplate (1.0m) and SEM Section
30	1000 A	1500 A	Electroplate (1.0m) and SEM Section
31	1500 A	500 A	SEM Section
32	1500 A	500 A	Electroplate (1.0m) and SEM Section
33	1500 A	500 A	Electroplate (1.0m) and SEM Section
34	1500 A	500 A	Electroplate (1.0m) and SEM Section
35	1500 A	500 A	Electroplate (1.0m) and SEM Section
36	1500 A	1000 A	SEM Section
37	1500 A	1000 A	Electroplate (1.0m) and SEM Section
38	1500 A	1000 A	Electroplate (1.0m) and SEM Section
39	1500 A	1000 A	Electroplate (1.0m) and SEM Section
40	1500 A	1000 A	Electroplate (1.0m) and SEM Section
41	1500 A	1500 A	SEM Section
42	1500 A	1500 A	Electroplate (1.0m) and SEM Section
43	1500 A	1500 A	Electroplate (1.0m) and SEM Section
44	1500 A	1500 A	Electroplate (1.0m) and SEM Section
45	1500 A	1500 A	Electroplate (1.0m) and SEM Section

Exhibit J



Experiment 6

Determine if marginal PVDseed layer step coverage can be improved by supplementary electroless deposition.

Barrier: Ta or TaN, 150A thickness

Seed layer : PVD Cu; thickness splits : 500A, 1000A, 1500A

Number of wafers per seed layer thickness : 15 (to allow for some trial-and-error process development in the following electroless deposition process)

Electroless deposition process targets : Add 500A, 1000A, 1500A of Cu (up to 5 wafers each per seed thickness)

Total number of wafers : 45

Following electroless deposition, one wafer per seed layer /electroless supplen thickness combination will be sectioned for SEM analysis. The remaining wal will be processed through a baseline Cu electroplating recipe, consisting of Enthone-OMI CU BATH M with additives, and FWD pulse plating at nominal parameters. Wafers will be sectioned to determine gap fill characteristics and ..... morphology. XRD should be performed to determine crystallinity and orientation.

PVD (INTEL
CVD (LETI

Experiment to Evaluate Electroless Cu Supplement of CVD Seed Layer

Evaluate Gap Fill, Grain Morphology

Wafer #	Seed Layer Thickness	Electroless Cu Thickness	Post-processing
1	500 A	500 A	SEM Section / Semitool
2	500 A	500 A	Electroplate (1.5m) and SEM Section / Semitool
3	500 A	500 A	Electroplate (1.0m) and SEM Section /INTEL
4	500 A	500 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
5	500 A	500 A	Electroplate (1.5m) and Damascene CMP / INTEL
6	500 A	1000 A	SEM Section / Semitool
7	500 A	1000 A	Electroplate (1.5m) and SEM Section / Semitool
8	500 A	1000 A	Electroplate (1.0m) and SEM Section /INTEL
9	500 A	1000 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
10	500 A	1000 A	Electroplate (1.5m) and Damascene CMP / INTEL
11	500 A	1500 A	SEM Section / Semitool
12	500 A	1500 A	Electroplate (1.5m) and SEM Section / Semitool
13	500 A	1500 A	Electroplate (1.0m) and SEM Section /INTEL
14	500 A	1500 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
15	500 A	1500 A	Electroplate (1.5m) and Damascene CMP / INTEL
16	1000 A	500 A	SEM Section / Semitool
17	1000 A	500 A	Electroplate (1.5m) and SEM Section / Semitool
18	1000 A	500 A	Electroplate (1.0m) and SEM Section /INTEL
19	1000 A	500 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
20	1000 A	500 A	Electroplate (1.5m) and Damascene CMP / INTEL
21	1000 A	1000 A	SEM Section / Semitool
22	1000 A	1000 A	Electroplate (1.5m) and SEM Section / Semitool
23	1000 A	1000 A	Electroplate (1.0m) and SEM Section /INTEL
24	1000 A	1000 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
25	1000 A	1000 A	Electroplate (1.5m) and Damascene CMP / INTEL
26	1000 A	1500 A	SEM Section / Semitool
27	1000 A	1500 A	Electroplate (1.5m) and SEM Section / Semitool
28	1000 A	1500 A	Electroplate (1.0m) and SEM Section /INTEL
29	1000 A	1500 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
30	1000 A	1500 A	Electroplate (1.5m) and Damascene CMP / INTEL
31	1500 A	500 A	SEM Section / Semitool
32	1500 A	500 A	Electroplate (1.5m) and SEM Section / Semitool
33	1500 A	500 A	Electroplate (1.0m) and SEM Section /INTEL
34	1500 A	500 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
35	1500 A	500 A	Electroplate (1.5m) and Damascene CMP / INTEL
36	1500 A	1000 A	SEM Section / Semitool
37	1500 A	1000 A	Electroplate (1.5m) and SEM Section / Semitool
38	1500 A	1000 A	Electroplate (1.0m) and SEM Section /INTEL
39	1500 A	1000 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
40	1500 A	1000 A	Electroplate (1.5m) and Damascene CMP / INTEL
41	1500 A	1500 A	SEM Section / Semitool
42	1500 A	1500 A	Electroplate (1.5m) and SEM Section / Semitool
43	1500 A	1500 A	Electroplate (1.0m) and SEM Section /INTEL
44	1500 A	1500 A	Electroplate (1.5m) and Evalute Grain Morphology / INTEL
45	1500 A	1500 A	Electroplate (1.5m) and Damascene CMP / INTEL

Barrier / Seed Layer Development

Experiments in Progress or Planning

Intel

Experiment to supplement PVD Cu seed with electroless Cu

Experiment to evaluate Ti, TiN, W, Ni, Al as platable seed/barrier layers

LETI

Experiment to suplement CVD Cu seed with electroless Cu

NCSU

Experiment to evaluate alternate PVD Cu seed deposition method

Independent

Experiment to determine if electroless Cu can be deposited reliably on activated TiN surface
Source of wafers : Sematech CMP Project

Experiment to evaluate Ir as platable barrier

Exhibit K

Advanced Technology Group

Meeting

9 am

Fri., May 2, 1997

Executive Lunch Rooms -East/West

Agenda

	Presenter	Project
9:00 - 9:10	Jeff Turner	Lab Scheduling and Resources
9:10 - 9:20	Tom Ritzdorf	Physical Parameter DOE -Experimental Design -Status and Plans
9:20 - 9:30	Kevin Coyle	Simplified Cu Electrolyte DOE -Experimental Design -Status and Plans
9:30 - 9:40	Tom Taylor	Seed/Barrier Layer Develop. -Experimental Design -Status and Plans Intel Mtg Update/Results
9:40 - 9:50	Lindy Graham	Investigation of Additive/Waveform Interactions in P.O.R. -INTEL Experimental Design
9:50 - 10:00	Bob Betz	Field ECD Process Support Plans

Exhibit L

SEMITOOL®

Metallization Process Group
655 West Reserve Drive, PO Box 7010, Kalispell, MT 59904 Phone: 406-752-2107 Fax: 406-752-5522

FAX COVER SHEET

To: Dr. Shu Jin / Intel — Fax# (408) 765-2949

From: Tom Taylor — Phone#: 406-752-2107, Fax#: 406-755-3226

Date: May 23, 1997

Subject: Experiment 6 / Rev 2 — Pages Including Cover: 2

Hello, Shu.

Hopefully we'll get a chance to talk about the structure of Experiment 7 (as I'm calling the work described in your fax of May 20) rather than just exchange voice mail messages.

For your consideration, I've revised the structure of Experiment 6, per the discussions of last week, which included yourself, myself, and Dr. Ruth Brain. Please note that I've reduced the total wafer requirement to 15 wafers, as we had tentatively agreed. The structure of the experiment is 'analyzable' with a standard statistics package. I'd like to have all fifteen wafers available at the outset of the work, but will understand if you prefer to send only wafers # 11 - 14 initially to provide a few set-up runs and gauge feasibility. Even if you send all wafers together, my intention is to run only these few wafers first; if initial results are completely lacking in promise, I would stop before consuming the remainder to no purpose.

Thanks. If for any reason we miss speaking to each other this afternoon, I hope you have a great Memorial Day holiday.

Best Regards,

Tom Taylor

EXHIBIT 1054

Page 1 of 2

ST003062

Experiment 6

Rev. 2

5/23/97

Wafer #	Seed Layer Thickness	Electroless Cu Thickness		Post-processing
1	500	500		SEM section after Electroless
2	"	"		Electroplate 1.0 micron Cu; SEM section
3	500	1000		SEM section after Electroless
4	"	"		Electroplate 1.0 micron Cu; SEM section
5	1000	500		SEM section after Electroless
6	"	"		Electroplate 1.0 micron Cu; SEM section
7	1000	1000		SEM section after Electroless
8	"	"		Electroplate 1.0 micron Cu; SEM section
9	750	500		Electroplate 1.0 micron Cu; SEM section
10	"	"		
11	750	750		SEM section after Electroless
12-14	"	"	x3	Electroplate 1.0 micron Cu; SEM section
15	750	1000		Electroplate 1.0 micron Cu; SEM section

Exhibit M

SEMITOOL®

Metallization Process Group
655 West Reserve Drive, PO Box 7010, Kalispell, MT 59904 Phone: 406-752-2107 Fax: 406-752-5522

FAX COVER SHEET

To: Dr. Shu Jin / Intel — **Fax# (408) 765-2949**

From: Tom Taylor — **Phone#: 406-752-2107**
Fax#: 406-755-3226

Date: May 27, 1997

Subject: Experiment 6 / Rev 2 — **Pages including Cover: 2**

[Following text is copied from a fax originally transmitted on Friday, May 23, but not received]

Hello, Shu.

Hopefully we'll get a chance to talk about the structure of Experiment 7 (as I'm calling the work described in your fax of May 20) rather than just exchange voice mail messages.

For your consideration, I've revised the structure of Experiment 6, per the discussions of last week, which included yourself, myself, and Dr. Ruth Brain. Please note that I've reduced the total wafer requirement to 15 wafers, as we had tentatively agreed. The structure of the experiment is 'analyzable' with a standard statistics package. I'd like to have all fifteen wafers available at the outset of the work, but will understand if you prefer to send only wafers # 11 - 14 initially to provide a few set-up runs and gauge feasibility. Even if you send all wafers together, my intention is to run only these few wafers first; if initial results are completely lacking in promise, I would stop before consuming the remainder to no purpose.

Thanks. If for any reason we miss speaking to each other this afternoon, I hope you have a great Memorial Day holiday.

Best Regards,

Tom Taylor

EXHIBIT
10516

Recommended experimental strategies

1) Follow-up on incremental deposition work. Should include pre-plating SE section of seed layer thickness. Recommend 1500A Cu on Ta or TaN barrier.
(20 wafers)

Concentration on FWD pulse plating
Deposition thicknesses of :

1000 A DC, FWD, PR
1500 A FWD
2000 A DC, FWD, PR
2500 A FWD
3000 A DC, FWD, PR
3500 A FWD
4000 A DC, FWD, PR
6000 A FWD
8000 A DC, FWD, PR

2) Experiment to explore the interaction between pulse plating parameters and electrolyte chemistry.
(50 wafers)

Bath 1 : Standard CU-BATH M with brighteners and levellers/suppressors

Bath 2 : CU-BATH M with brightening agents only (two concentrations, 50% & 100%)

Bath 3 : CU-BATH M with suppressors only (two concentrations, 50% & 100%))

Bath 4 : CuSO4/H2SO4 "Semitool Basic Bath"

Waveforms to include :

DC plating at two different current densities

FWD plating at two different conditions (modify pulse width/amplitude) and two time averaged current densities – preferrably the same as employed for DC. One condition should be equivalent to the conditions previously used for Intel samples.

Pulse-reversed waveforms. Based on results obtained in STI DOE.

3) Experiment to determine if seed layer continuity on feature sidewalls can be supplemented with electroless Cu.

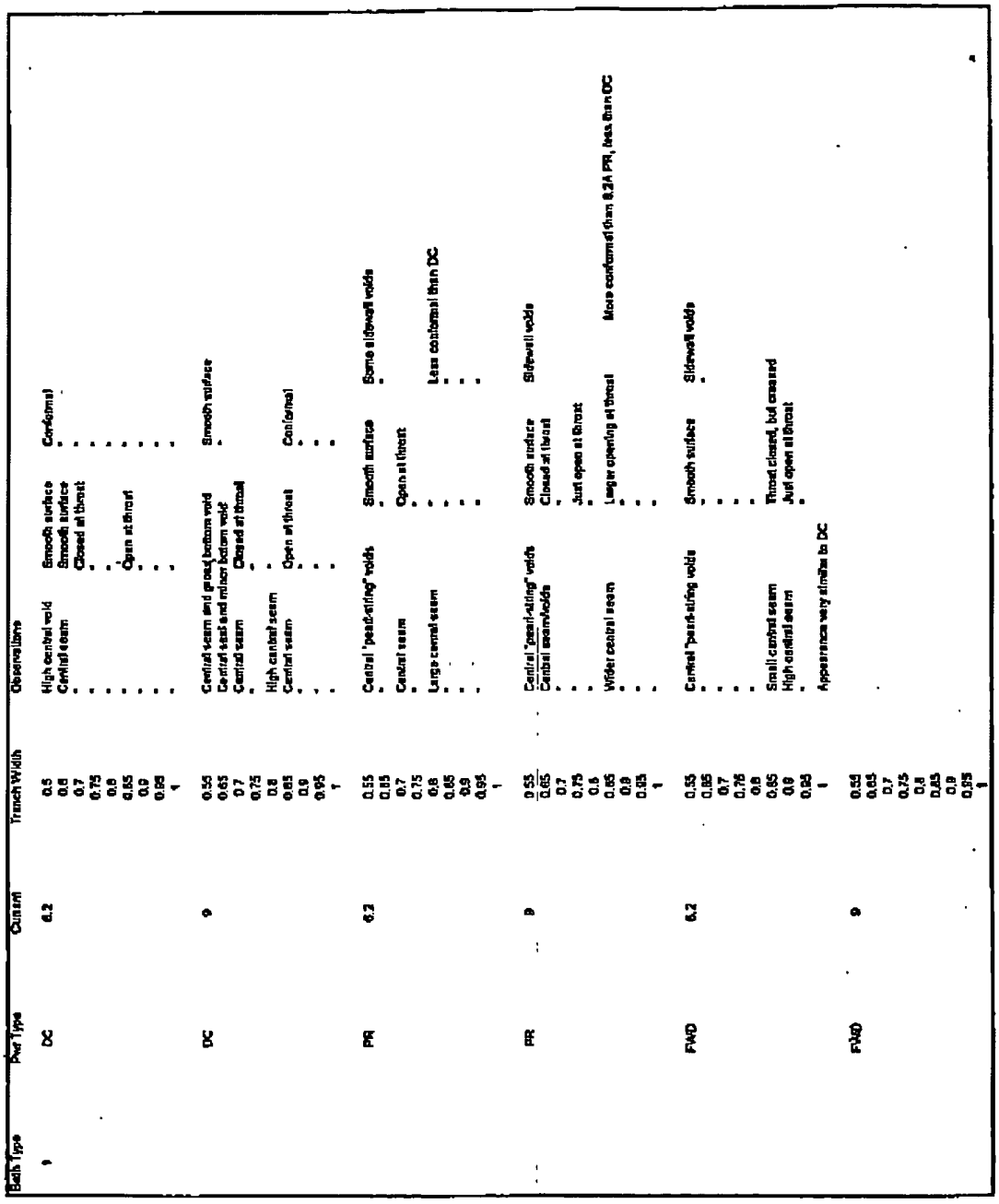
Barrier Material : Ta or TaN, 150A thickness

Seed layer thicknesses : 500A, 1000A, 1500A

Number of wafers per seed layer thickness : 15

Total number of wafers : 45

Electroless deposition process targets : Add 500A, 1000A, 1500A of Cu (5 wafers each per seed thickness)



Bath Type	Pwr Type	Current	Trench Width	Observations		
1	DC	0.2	0.5	High central void	Smooth surface	Conformal
			0.6	Central seam	Smooth surface	
			0.7		Closed at throat	
			0.75			
			0.8			
			0.85		Open at throat	
			0.9			
			0.95			
			1			
	DC	0	0.55	Central seam and grass bottom void	Smooth surface	
			0.65	Central seam and minor bottom void		
			0.7	Central seam	Closed at throat	
			0.75			
			0.8	High central seam		
			0.85	Central seam	Open at throat	Conformal
			0.9			
			0.95			
			1			
	FR	0.2	0.55	Central "peak-sting" voids	Smooth surface	Some sidewall voids
			0.65			
			0.7	Central seam	Open at throat	
			0.75			
			0.8	Large central seam		Less conformal than DC
			0.85			
			0.9			
			0.95			
			1			
	FR	0	0.55	Central "peak-sting" voids	Smooth surface	Sidewall voids
			0.65	Central seam/voids	Closed at throat	
			0.7			
			0.75		Just open at throat	
			0.8			
			0.85	Wider central seam	Larger opening at throat	More conformal than 0.2A FR, less than DC
			0.9			
			0.95			
			1			
	FWD	0.2	0.55	Central "peak-sting voids	Smooth surface	Sidewall voids
			0.65			
			0.7			
			0.75			
			0.8			
			0.85	Small central seam	Throat closed, but creased	
			0.9	High central seam	Just open at throat	
			0.95			
			1	Appearance very similar to DC		
	FWD	0	0.55			
			0.65			
			0.7			
			0.75			
			0.8			
			0.85			
			0.9			
			0.95			
			1			

Bath 1

Page 1

Bath Type	Pwr Type	Current	Trench Width	Observations		
7	DC	6.2	0.5	Central void	Few sidewall voids	Smooth surface
			0.6	Central void/seams		"
			0.7	Central seam	Closed at throat	
			0.75	"	"	
			0.8	"	"	
			0.85	"	"	
			0.9	Central seam	Just open at throat	
			0.95	"	"	
			1	"	"	
	DC	9	0.55	Gross sidewall/bottom voids		Smooth surface
			0.65	Central seam and minor sidewall/bottom void*		
			0.7	Central seam	Closed at throat	
			0.75	"	"	
			0.8	Central "pearl-string" v*		
			0.85	Central seam	Open at throat	Conformal
			0.9	"	"	"
			0.95	"	"	"
			1	"	"	"
	PR	6.2	0.55	Central "pearl-string" voids	Smooth surface	Gross sidewall/bottom voids
			0.65		"	"
			0.7	Central seam	Open at throat	
			0.75	"	"	
			0.8	Large cerval seam	"	Less conformal than DC
			0.85	"	"	"
			0.9	"	"	"
			0.95	"	"	"
			1			
	PR	9	0.55	Central seam/voids	Smooth surface	Gross bottom/sidewall voids
			0.65	"	Closed at throat	"
			0.7	"	"	
			0.75	"	Just open at throat	
			0.8	"	Larger opening at throat	
			0.85	Wider central seam	"	Same as 6.2A PR
			0.9	"	"	
			0.95	"	"	
			1	"	"	
	FWD	6.2	0.55	Slight central voids	Smooth surface	Sidewall/bottom voids
			0.65	Central seams	"	"
			0.7	Central seams	"	
			0.75	"	"	
			0.8	"	"	
			0.85	Larger central seam	Just open at throat	
			0.9	"	Open at throat	
			0.95	"	"	
			1	Appearance very similar to DC		
	FWD	9	0.55			
			0.65			
			0.7			
			0.75			
			0.8			
			0.85			
			0.9			
			0.95			
			1			

Bath Type	Pwr Type	Current	Trench Width	Observations		
3	DC	6.2	0.55	Large central seam	Thick Cu on mesa	Large divit at trench top
			0.65	Central seam	"	"
			0.7	Central seam	Open at throat	Nonconformal dep; thick on mesa
			0.75	"	"	"
			0.8	Seam terminates at half trench height		Nonconformal, witless-entrant
			0.85	"	"	"
			0.9	"		"
			0.95	"		"
			1	Seam terminates at one-third height		Re-entrant
	DC	9	0.55	Large central seam		Large divit
			0.65	"		Divit / "pinch-off"
			0.7	Central seam	Open at throat	Nonconformal
			0.75	Seam terminates at two-thirds height		Slight re-entrant
			0.8	Seam terminates at half height		Slight re-entrant
			0.85	Seam terminates at half height		Re-entrant Low central void
			0.9	"		"
			0.95	"		"
			1	Seam terminates at one-third height		"
	PR	6.2	0.55	Central seam	Rougher surface	Sidewall voids
			0.65	"	"	Large surface divit
			0.7	"Pearl-string" voids	"	Closed at throat
			0.75	Central seam	"	Just open at throat
			0.8	Large divit	"	Open at throat; nonconformal
			0.85	"	"	"
			0.9	Seam terminates at two-thirds height		"
			0.95	"	"	"
			1	Seam terminates at half height	"	
	PR	9	0.55	Central "pearl-string"	Rougher surface	Sidewall voids
			0.65	"	Closed at throat	Non-conformal(?),
			0.7	Central seam	"	Large divit
			0.75	"	"	"
			0.8	"	Larger opening at throat	
			0.85	Seam terminates at 3/4 height	"	
			0.9	"	"	
			0.95	Seam terminates at two-thirds height		
			1	"	"	
	FWD	6.2	0.55	Large central voids (low, triangular)		Large divit / "pinch-off"
			0.65	"		"
			0.7	Large central seam	Open at throat	Non-conformal, thick on mesa
			0.75	"	"	Re-entrant
			0.8	"	"	Very re-entrant
			0.85	"	"	"
			0.9	"	Keyholed	
			0.95	"	"	
			1	"	"	
	FWD	9	0.55			
			0.65			
			0.7			
			0.75			
			0.8			
			0.85			
			0.9			
			0.95			
			1			

Bath Type	Pwr Type	Current	Trench Width	Observations	Dendrite	Cross bottom/sidewall voids
4	DC	4.2	0.55	Large central seam	Dendrite	Cross bottom/sidewall voids
			0.65	Central seam		Slight sidewall voids
			0.7	"Pearl-string"		Thin on mesa; divot at throat
			0.73	Central seam		
			0.8	"Pearl-string"	Dendrite at trench mouth	
			0.85	Central void cloud	Dendrite at trench mouth	
			0.9		Porous Cu in bench	Large divot; thin on mesa
			0.95			
			1	Open at trench mouth; very non-conformal	thick at bench bottom	Re-entrant
	DC	6	0.55	Central seam	Grass dendrites	Grass bottom/sidewall voids
			0.65			Very thin on mesa
			0.7	Central seam		Thin on mesa
			0.75	Central seam		
			0.8	Central seam / porous Cu		Same as above
			0.85	Void clouds / porous Cu		
			0.9			
			0.95			
			1			
	FR	6.2	0.55	Central seam	Spiky dendrites	Mose conformal (?)
			0.65			Just open at throat
			0.7			Triangular opening at throat
			0.73			
			0.8	Deep seam		Large triangular opening at throat
			0.85			
			0.9			
			0.95	Deep seam	Spiky, globular dendrites	Thin Cu, but conformal
			1			
	FR	9	0.55	Central seam	Small spiky dendrites	
			0.65			Closed at throat; bulb with divot
			0.7	Central seam		Large triangular divot at throat
			0.75			
			0.8	Deep central seam		
			0.85		Huge globular dendrites	
			0.9			
			0.95			
			1			
	FWD	4.2	0.55			
			0.65			
			0.7			
			0.75			
			0.8			
			0.85			
			0.9			
			0.95			
			1			
	FWD	9	0.55	"Pearl-string" voids	Rougher surface; dendrites(?)	Conformal; closed at throat
			0.65		Small spiky dendrites	
			0.7		Rougher surface	
			0.75			Porous Cu
			0.8			
			0.85			
			0.9	Central seam		Just closed at throat
			0.95			
			1	Deep central seam		Just open at throat

Bath 1

Page 1

Bath 3

Bath Type	Part Type	Curved	Trench Width	Observations		
3	DC	0.2	0.55	High central seam	Smooth surface	Slightly thicker on mesa
			0.65	Slight central seam		
			0.7	Slight central seam		
			0.75	No seam visible		
			0.8			
			0.85			
			0.9			
			0.95			
			1	No seam; completely filled		
	DC	0	0.55	High central seam	Sndpoth surface	Slightly thicker on mesa
			0.63	Central seam		
			0.7	Slight central seam		
			0.75	No seam visible		
			0.8	High central "wildfire"		
			0.85	No seam visible		
			0.9	Central "welder"		
			0.95			
			1	No seam; completely filled		
	PR	0.2	0.55	Central seam	Open at throat	Smooth surface; conformal dep
			0.65	"Pearl-strings"	Just closed at throat	
			0.7	Central seam	Open at throat (half filled)	
			0.75	Central seam	One-third filled	
			0.8			
			0.85		One-fourth filled	
			0.9			
			0.95			
			1			
	PR	0	0.55	Central seam	Open at throat	Smooth surface; conformal dep
			0.63	"Pearl-strings"	Just closed at throat	
			0.7	"Welder"	Closed at throat	Divot at throat
			0.75	No welds visible	3/4 Filled	Large chip
			0.8	No welds visible	2/3 Filled	
			0.85			
			0.9		1/2 filled	Slightly thinner on sidewalls
			0.95		1/3 filled	
			1			
	FWD	0.2	0.53			
			0.65			
			0.7			
			0.75			
			0.8			
			0.85			
			0.9			
			0.95			
			1			
	FWD	0	0.55	High central seam	Smooth surface	Slightly thicker between masses
			0.65			
			0.7	No seam visible		
			0.75			
			0.8			
			0.85			
			0.9			
			0.95			
			1			

Page 1

Experiment #	Dates	# Wafers	Wfr Size	Purpose	Conclusions
6	Early June	15	200mm	Seed supplement with electroless Cu Seed thicknesses of 500Å, 750Å, 1000Å Electroless Cu thickness of 500Å - 1000Å Electrolytic dep of 1.0µm	Pending; first 'set-up' wafers arrived at STI 6/2/97
7	TBD	TBD	200mm	Evaluation of low-frequency pulse Form of in-situ electropolish Relies on dep-etch sequence	Pending
8	05/12/1997	12	150mm	Evaluation of FWD, DC, PR waveforms Blanket and patterned wafers, TIN Barrier Other purposes unknown to STI	Waiting results
9	05/16/1997	18	200mm	Investigation of CVD Cu seed (500Å - 1500Å) Pre-clean' splits prior to barrier/seed DC/FWD, PR waveforms	Waiting results
10	05/28/1997	10	200mm	DOE over the factors of Waveform (FWD, PR) Peak Current (4.5, 5.3, 6.2A) Bath temp (15, 20, 25 deg. C) Brightener Conc. (50, 100, 150%)	Waiting results
11	06/03/1997	9	200mm	Evaluation of DC, FWD, PR TIN Barrier	Pending

Total Wafers to Date : 165

Hardware Generation Roadmap

Semitool Cu ECD Systems

	Feasibility/Development Tools 1995 -> 1996	IRONMAN Tool Generation 1 1996 -> 1997	Production Tool Generation 2 1997 -> 1998	300mm ECD 1998 -> 1999	300mm ECD 1999 -> 2000	300mm ECD 2000 -> 2001
Flow Rate Range	2 - 8 gpm	2 - 9 gpm	1 - 10 gpm	1 - 10 gpm	1 - 10 gpm multi-step programmable	1 - 10 gpm multi-step programmable
Flow Variation Chamber-to-chamber	0.5 gpm	0.5 gpm	0.2 gpm	0.2 gpm	0.1 gpm	0.1 gpm
Electrolyte Temperature	25 +/- 5 deg. C	25 +/- 5 deg. C	40 +/- 20 deg. C	40 +/- 20 deg. C	40 +/- 20 deg. C	40 +/- 20 deg. C
Max. Temperature Variation Chamber-to-chamber	5 deg. C	5 deg. C	5 deg. C	2 deg. C	1 deg. C	1 deg. C
Power Supply Range Continuous/Peak	30A / 100A Endpoint on integrated current	30A / 100A Endpoint on integrated current	TBD Endpoint on integrated current	TBD Cell conductance monitor Endpoint on integrated current	TBD Cell conductance monitor Endpoint on plated thickness	TBD Cell conductance monitor Endpoint on plated thickness
Contact Type	Uncoated	Uncoated	Coated	Coated	Sealed/Remote	Sealed/Remote (seed layer enhancement)
Contact Resistance Sensing	None	None	None	In-situ cell voltage sensing	In-situ contact resistance sensing	In-situ contact sensing and biasing
Bath Analysis/ Replenishment	None	Off-line analysis Manual replenishment	Off-line analysis Open loop replenishment	On-line analysis Open-loop replenishment	On-line analysis Feedback-controlled replenishment	On-line analysis Feedback-controlled replenishment
Wafer / Electrolyte Interface Control	Meniscus plating Manual Set-up	Meniscus Plating Manual Set-up	Meniscus plating Metered Stops	Meniscus plating Metered Stops Electrolyte contact sensing	Meniscus plating Programmable stops Electrolyte contact sensing	Wfr edge & backside protection Programmable stops Electrolyte contact sensing
Fluid Flow Path	Anode perimeter	Anode perimeter	Anode perimeter	Anode perimeter	Anode/chamber perimeter	Anode/chamber perimeter
Anode Configuration	Inert anode	Consumable anode	Consumable anode w/ shield	Consumable anode w/ shield	Consumable anode Optimized configuration	Consumable anode Optimized configuration
Auxiliary Electrodes	None	None	Auxiliary cathode Single segment	Auxiliary cathode Multi-segment	Auxiliary cathode Multi-segment	Auxiliary cathode Multi-segment
Diffuser type	Perforated plate	Perforated plate	Perforated plate	Alternative materials Mesh-type	Mesh-type, or none	Mesh-type, or none
Electrolyte Filtration	In-line	In-line	In-line	In-line plus point-of-use	In-line plus point-of-use	In-line plus point-of-use

Exhibit N

SEMITOOL®

Advanced Technology Process Group
655 West Reserve Drive, PO Box 7010, Kalispell, MT 59904 Phone: 406-752-2107 Fax: 406-752-3522

To: Shu Jin, Chun Mu (INTEL)
From: Matt Johnson
Date: 6/30/97
Subject: Seedlayer enhancement through electroless plating.
cc: Henry Stevens, Bob Berner, Jeff Turner, Linlin Chin

Experiment:

Investigation of electroless plating in combination with ECD for trench/via filling applications.

Process Details:

The electroless bath used was a basic copper sulfate solution with formaldehyde and EDTA used as activation agents. The ECD was performed using a standard commercially available copper make-up solution and a forward only pulse type wave form. Five wafers were plated and the resulting deposition was observed using SEM photography. The following table is a summary of the plating processes used for each wafer.

wafer ID	electroless (Å)	ECD (µm)	prewet
335	750	1.5	no
341	no	1.5	no
381	750	no	no
383	750	1.5	yes
387	1500	1.5	yes

Wafer 381 was initially plated using the electroless deposition only for a total bath time of 2.5 minutes. Photographs labeled SEM 1 and 2 are of this wafer and show an even deposition layer covering the trenches and vias that is approximately 750 Å. The sputtered copper layer and the electroless copper layer can also be distinguished in the photographs.

Wafer 335 was also electroless plated to the nominal thickness of 750 µm and then plated using ECD. Photographs labeled SEM 3 and 4 are of this wafer. The structures on this wafer larger than approximately 0.7 µm wide were well filled with no voids. Trenches less than 0.7 µm wide appear to have developed pin-hole structures as a result of the trenches being shut off before complete deposition has occurred.

Wafer 341 was electroplated only and also appears to have good filling characteristics in the larger trenches as shown in photographs SEM 5 and 6. Some of the smaller structures on this

wafer exhibit some voids on the walls of the trenches which may be characteristic of seed layer discontinuities, particularly near the bottoms of the trenches.

As a result of the SEM photographs obtained of wafer 381 in which the seed layer and electroless layer were distinguishable by a small barrier, wafers 383 and 387 were prewet for 10 sec in the acid copper make-up solution and then run in an SRD to remove any oxide that may have been present. It is suspected that this prewet step had a negative effect on the electroless and ECD steps as the 10 sec prewet may have removed portions of the existing seed layer to an extent where enhancement through electroless plating was not effective. Photographs labeled SEM 7 and 8 are of voids in the trenches of wafers 383 and 387 respectively. Wafer 387 has the largest voids of the two wafers.

Summary:

Electroless plating was used to enhance the seedlayer of four experimental wafers with some success. The SEM photographs taken of the electroless layer show a uniform enhanced seedlayer in all size trenches and vias. The ECD in combination with the electroless deposition also exhibits good filling capabilities with the exception of pin-holes structures in the smallest trenches and vias.

If you have questions regarding this experiment or future electroless plating experimentation. I can be reached by phone here at Semitool at (406) 752-2107 ex. 7271.

Best Regards,

Matt Johnson

Exhibit O

Atto...., Docket No. 291958171US02
Semitool Ref No. P98-0025US3

Express Mail Label _

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as Express Mail No. EL099017980US in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on:

Date:_____ By:_____

Melody J. Almberg

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE PATENT APPLICATION NO.:	6,197,181
APPLICATION NO.:	09/045,245
FILED:	MARCH 20, 1998
ISSUED:	MARCH 6, 2001
FOR:	**METHOD FOR ELECTROLYTICALLY DEPOSITING METAL ON A MICROELECTRONIC WORKPIECE**

Declaration of Harry M. Cross, Jr. In Support of Joint Inventorship

1. I, Harry M. Cross, Jr., am Corporate Counsel of Semitool, Inc. (Semitool) located in Kalispell, Montana.

2. Based upon recently discovered documentary evidence, and recent statements from Mr. Thomas Taylor (Taylor) and Mr. Lin Lin Chen (Chen), Taylor is a co-inventor of (a) certain subject matter claimed U.S. Patent No. 6,197,181 ("the '181 Patent") and (b) subject matter claimed in U.S. Application No. 10/302,711 as set forth in the Preliminary Amendment filed on November 22, 2002.

3. In April 1997, Taylor was a team leader within the Advanced Technology Group ("ATG") of Semitool, and he was involved with developing new technologies for improving seed layers.

4. On April 4, 1997, the Semitool ATG group held a meeting that included a discussion of Semitool's current developments in seed layer technology. During this

meeting, Taylor presented information about Semitool's efforts to improve and optimize seed layers by using an electroless process to perform seed layer enhancement. According to Taylor, the seed layers to be enhanced were thin seed layers in the range of 200-500Å, and the purpose of the electroless enhancement process was to fix deficiencies (i.e., voids and discontinuities) in the seed layer before using an electroplating procedure to bulk fill copper on the seed layer.

5. After April 4, 1997, Taylor designed experiments to demonstrate the electroless enhancement process to Intel Corporation (Intel). On May 1, 1997, Taylor sent a confidential memorandum to Intel regarding his proposal to supplement the step coverage of PVD seed layers by a short electroless copper deposition process before beginning electrolytic plating. Between May 1 and June 30, 1997, Semitool performed the electroless seed layer enhancement experiments designed by Taylor.

6. Semitool prepared a confidential report dated June 30, 1997, regarding the experiments designed by Taylor. The results of these experiments established that the electroless process designed by Taylor was effective in eliminating deficiencies in seed layers for structures having a width larger than approximately 0.7 μm.

7. Although the electroless procedures designed by Taylor successfully repaired defective seed layers with certain characteristics, and although they also showed promise of greater success with further development, Semitool decided to devote its resources to other priorities.

8. Chen, the sole inventor named in the '181 Patent, began working for Semitool on April 14, 1997. Chen was not present at the ATG group meeting on April 4, 1997, but he later received a copy of the June 30, 1997, report describing Taylor's electroless seed layer enhancement experiment. Chen received a copy of this report to bring him up to speed on Semitool's current activities regarding seed layers and to solicit his feedback for improvements regarding Semitool's research and development activities.

9. In the middle of 1997, Taylor transferred from the Semitool ATG group to the Semitool marketing department. Taylor did not have direct involvement with developing processes for enhancing seed layers after this time.

10. In September 1997, I joined Semitool as a part-time consultant for three days a week.

11. In November 1997, Mr. Robert Berner, Corporate Vice President of Technology for Semitool, terminated his employment with Semitool to work for a different company. Although Mr. Berner was made aware of Taylor's previous work regarding electroless processing of seed layers, he did not inform me of Taylor's earlier work in the short time that we were both at Semitool. Also, after leaving Semitool, Berner was not available to assist me in coordinating the intellectual property of Semitool.

12. In late 1997, Chen began focusing on methods to fix deficiencies in seed layers. On December 22, 1997, Chen conceived of an electrolytic seed layer repair process, which is the preferred embodiment of the invention described in the '181 Patent.

13. The application for the '181 Patent was filed on March 20, 1998. Although certain claims in the '181 Patent cover electroless processing of a deficient seed layer, Taylor was inadvertently not named as an inventor on the application for the '181 patent.

14. On May 1, 1998, after (a) Taylor had transferred to marketing, (b) Berner had left Semitool, and (c) the application for the '181 Patent had been filed, I became a full-time employee of Semitool and assumed full responsibility for Semitool's intellectual property. Because of the personnel and organizational changes at Semitool involving Taylor and Berner in mid to late 1997, and also because of my being a part-time consultant from September 1997 to May 1, 1998, Semitool simply inadvertently lost track of the work that Taylor and Semitool had performed using an electroless process to enhance deficient seed layers.

15. I only recently became aware and confirmed that Taylor had made an inventive contribution to seed layer the repair processes covered in certain claims of '181 Patent and U.S. Application No. 09/694,413.

16. After allowance of several claims in U.S. Application No. 09/694,413, Semitool cancelled claims in that application which were jointly invented by Taylor and Chen, and only allowed subject matter invented solely by Chen to proceed to allowance.

17. Semitool is pursuing the allowed and subsequently cancelled claims from U.S. Application No. 09/694,413 that were jointly invented by Chen and Taylor in U.S. Application No. 10/302,711.

18. Based on the foregoing, the error in inventorship of failing to name Taylor as a joint inventor of certain claimed subject matter of the '181 Patent occurred without any deceptive intention on the part of Taylor, Chen or others involved with the prosecution of the '181 Patent or U.S. Application No. 09/694,413.

19. I declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that all statements were made with the knowledge that making willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Attorney Docket No. 291958171US02
Semitool Ref No. P98-0025US3

This Declaration is executed on the ____ day of May, 2003.

Date: 5/22/03

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